AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method, comprising:

forming a first dielectric layer on a semiconductor substrate;

depositing a first polysilicon layer above the dielectric layer;

introducing dopant atoms of a first type of dopant material into the first polysilicon layer during the deposition process;

forming a second layer above the first polysilicon layer, wherein the second layer is doped with a second type of dopant material that is opposite the first type of dopant material in the first layer;

forming a second dielectric layer above the second layer;

forming a control gate above the second dielectric layer; and

forming a source and a drain in the substrate such that the first polysilicon layer overlaps the source and the drain.

2-4. (Canceled)

5. (Currently Amended) The method of claim 1, wherein forming the second layer comprises forming a second polysilicon layer above the first polysilicon layer such that the second layer overlaps the source and the drain.

6. (Original) The method of claim 5, wherein forming the second polysilicon layer comprises depositing the second polysilicon layer and introducing dopant atoms of the second type of dopant material into the second polysilicon layer during the deposition process.

7. (Original) The method of claim 5, wherein forming the second polysilicon layer comprises performing an ion implantation process to introduce dopant atoms of the second type of dopant material into the second polysilicon layer.

8. (Previously Presented) The method of claim 1, further comprising forming a barrier layer between the first polysilicon layer and the second layer.

9-13. (Canceled)

14. (Previously Presented) The method of claim 8, wherein forming the barrier layer comprises forming the barrier layer having a thickness ranging from approximately 10-50 Å.

15. (Currently Amended) A method of forming a double-doped floating gate, comprising:

forming a first dielectric layer on a semiconductor substrate;

depositing a first polysilicon layer above the first dielectric layer;

introducing dopant atoms of a first type of dopant material into the first polysilicon layer during the deposition process;

forming a barrier layer above the first polysilicon layer;

forming a second polysilicon layer above the barrier layer;

forming a second dielectric layer above the second polysilicon layer;

forming a control gate above the second dielectric layer; and

forming a source and a drain in the substrate such that the first polysilicon layer overlaps the source and the drain.

16. (Canceled)

17. (Previously Presented) The method of claim 15, wherein introducing dopant atoms of the first type of dopant material into the first polysilicon layer comprises introducing dopant atoms of the first type of dopant material into the first polysilicon layer to a first dopant concentration of approximately 10^{15} - 10^{20} atoms/cm^3.

18-19. (Canceled)

20. (Currently Amended) The method of claim 15, wherein forming the second polysilicon layer comprises depositing the second polysilicon layer such that the second polysilicon layer overlaps the source and the drain and introducing dopant atoms of the second type of dopant material into the second polysilicon layer during the deposition process.

21. (Original) The method of claim 20, wherein forming the second polysilicon layer comprises introducing dopant atoms of the second type of dopant material into the second polysilicon layer to a second dopant concentration of approximately 10^{18} - 10^{21} atoms/cm^3.

22. (Original) The method of claim 15, wherein forming the second polysilicon layer comprises performing an ion implantation process to introduce dopant atoms of the second type of dopant material into the second polysilicon layer.

23. (Original) The method of claim 22, wherein forming the second polysilicon layer comprises introducing dopant atoms of the second type of dopant material into the second polysilicon layer to a second dopant concentration of approximately 10^{18} - 10^{21} atoms/cm^3.

24-28. (Canceled)

29. (Withdrawn) An apparatus, comprising:

a first dielectric layer formed on a semiconductor substrate;

a double-doped floating gate formed above the dielectric layer;

a second dielectric layer formed above the double-doped floating gate;

a control gate formed above the second dielectric layer; and

a source and a drain formed in the substrate.

30. (Withdrawn) The apparatus of claim 29, wherein the double-doped floating gate comprises a first doped polysilicon layer formed above the first dielectric layer and a second doped polysilicon layer above the first polysilicon layer.

31. (Withdrawn) The apparatus of claim 30, wherein the first doped polysilicon layer is doped to a first dopant concentration of about 10^{15} to 10^{20} atoms/cm^3.

32. (Withdrawn) The apparatus of claim 31, wherein the second doped polysilicon layer is doped to a second dopant concentration of about 10^{18} to 10^{21} atoms/cm^3 with a dopant material having a dopant type opposite to that of the first dopant.

33. (Withdrawn) The apparatus of claim 30, wherein the second doped polysilicon layer is doped to a second dopant concentration of about 10^{18} to 10^{21} atoms/cm^3.

34. (Withdrawn) The apparatus of claim 29, wherein the double-doped floating gate comprises a barrier layer formed above the first polysilicon layer and below the second polysilicon layer.